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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,419	02/12/2004	Christopher H. Dick	X-1505 US	4321

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
PIERRE LOUIS, ANDRE	
ART UNIT	**PAPER NUMBER**
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,419	DICK ET AL.	
	Examiner	Art Unit	
	Andre Pierre-Louis	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-17 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-17 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 6/11/2007 has been received and fully considered; Claims 13,18-22, and 24 are cancelled; and claims 1-12, 14-17, and 23 are presented for examination.

2. Regarding the rejection under 35 USC 101, the Examiner withdraws the rejection in view of the amendment.

3. As per the claims' rejection under 35 USC 103, using Lin et al., the Examiner withdraws the rejection, render moot all Applicant's arguments with regards to Lin.

Claim Objections

4. Claims 15-17 are objected to because of the following informalities: the claims depends from a cancelled claim. Appropriate correction is required.

Response to Arguments

5. Applicant's arguments filed 06/11/2007 have been fully considered but they are moot, in view of the new rejection below. Regarding Applicant's assertion that the office action does not show that all the limitations are suggested by the combination of Lee and Cooke et al. and does not provide a proper motivation for modifying the teachings of Lee with teachings of Cooke; and that a prima facie case of obviousness has not been established, is acknowledged. However, the Examiner respectfully disagrees and notes that, although Cooke was brought in as a secondary for further support in the rejection of the instant claims, Lee does teaches the transferring of vector data between the block *(see pgs.32, 33,73,85-3, and ch.5),* which is further relied upon in the secondary reference. The Examiner further notes that the grounds of rejection below clearly shows a complete mapping of the cited prior art to the instant claims addressing all claims limitations, and that the Examiner, in the below grounds of rejection, points to specific

portion of the references for reasons/motivation to combine the references. Therefore, a prima facie has clearly been established and the Examiner has properly rejection the claims in accordance with the practices and procedures set forth in the MPEP.

6. While the Applicant believes that the independent claims along with their dependencies should be found allowable, the Examiner respectfully disagrees and asserts that the rejection clearly supports the Examiner's position in rejecting the instant claims.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7.0 Claims 1-12,14-17, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seungjun Lee (A Hardware-Software co-Simulation Environment, PHD Thesis University of California, Berkeley 1993), in view of Cooke et al. (U.S. Patent No. 6,968,514).

7.1 In considering the independent claims 1 and 23, Lee substantially teaches a method for transferring data between blocks in a design during simulation, comprising: determining a first buffer size in response to specification of a vector input port of a first high-level block of the design *(pgs.152-167);* determining a second buffer size in response to specification of a scalar input port of a second high-level block of the design *(pg.152-167);* co-simulating a first hardware-implemented block on a hardware co-simulation platform, wherein the first hardware implemented block implements the first high-level block in the design simulated in a high-level modeling system (HLMS) (*see section 1.3 (1.3.4)*; transferring a first vector of data values received by the first high-level block at the vector input port to the first hardware-implemented block via a single call to a first function provided by an interface that couples the HLMS to the first hardware implemented block (*see 1.3.4, 2.3.2, also see Ch. 5)*; wherein the first vector of data values fills the first buffer size *(pg.8-15,49-57, and 84-90)*; co-simulating a second hardware-implemented block on a hardware co-simulation platform, wherein the second hardware-implemented block implements the second high-level block in the design simulated in the (HLMS) (*see section 1.3 (1.3.4)*; accumulating a plurality of input scalar values received at the scalar input port in a second vector data values that fills the second buffer size, by the second high-level block *(see section 1.3)*; and transferring the second vector of data values from the first high-level block to the hardware-implemented block via a single call to the first function of the interface that couples the HLMS to the second hardware-implemented block (*see 1.3.4, 2.3.2, also see Ch. 5).* Although Lee does not clearly state the term transferring the data via a single first transfer instruction, he teaches transferring data from one block to another *(see 1.3.4, ch.5).* Nevertheless, Cooke et al. substantially teaches a Block Based Design

Methodology, which the transferring of data between multiple block of the design (*see col.35 lines 32-49*) and further teaches a burst data transferring using a bridge (*col.42 lines 55-63*), and further teaches accumulating data in a table form a matrix before transferring from one block to the other (*see col.35 lines 32-67.* Lee and Cooke et al. are analogous art because they are from the field of endeavor and that the method teaches by Cooke et al. is similar to that of Lee. Therefore, it would have been obvious to one ordinary skilled in the art at the time of the applicant's invention to combine the simulation method of Cooke et al. with the co-verification system and method of Lee because Cooke et al. teaches the advantage of using a method that provides a methodology for constructing re-usable circuit blocks which takes account of the special requirements of programmable components, and facilitates the integration of such programmable components with non-programmable components (*col.5 lines 32-48*).

7.2 With regards to claims 2 and 14, the combined teachings of Lee and Cooke et al. substantially teach the step of simulating operation of a third high-level block in the design (*see Lee section 2-3); and* transferring a first vector of data values from the third high-level block to the vector input port of the first high-level block (*see Lee 1.3.4, 2.3.2, also see Ch. 5; also see Cooke et al. col.35 lines 32-49 & col.42 lines 55-63).*

7.3 As per claims 3 and 15, the combined teachings of Lee and Cooke et al. substantially teach the step of co-simulating a third hardware-implemented block on a hardware co-simulation platform, wherein the third hardware, implemented block implements a third high-level block in the design simulated in the HLMS (*see Lee section 2-3);* and transferring a first vector of data values from the third high-level block to the vector input port of the first

high-level block (*see Lee 1.3.4, 2.3.2, also see Ch. 5; also see Cooke et al. col.35 lines 32-49 & col.42 lines 55-63).*

7.4 Regarding claim 4, the combined teachings of Lee and Cooke et al. substantially teach the step of transferring a third vector of data values received by the interface from the first hardware-implemented block, to the first high-level block in response to a single call to a second function provided by the interface and invoked by the first high-level block (*see Lee 1.3.4, 2.3.2, also see Ch. 5; also see Cooke et al. col.35 lines 32-49 & col.42 lines 55-63).*

7.5 With regards to claim 5, the combined teachings of Lee and Cooke et al. substantially teach the step of simulating operation of a third high-level block in the design in the HLMS (*see Lee section 2-3)*; and transferring the third vector of data values from the first high-level block to the second high-level block (*see Lee 1.3.4, 2.3.2, also see Ch. 5; also see Cooke et al. col.35 lines 32-49 & col.42 lines 55-63).*

7.6 As per claim 6, the combined teachings of Lee and Cooke et al. substantially teach the step of co-simulating a third hardware-implemented block on a hardware co-simulation platform, wherein the third hardware implemented block implements a third high-level block in the design simulated in the HLMS (*see Lee section 2-3)*; and transferring the second vector of data values from the first high-level block to the third high-level block (*see Lee 1.3.4, 2.3.2, also see Ch. 5; also see Cooke et al. col.35 lines 32-49 & col.42 lines 55-63).*

7.7 Regarding claim 7, the combined teachings of Lee and Cooke et al. substantially teach the step of that wherein the hardware co-simulation platform includes a field programmable gate array (FPGA), and the method further comprises: establishing a first buffer of the first buffer size and a second buffer size on the FPGA (*see Lee pgs 152-167; and also see*

Cooke et al. col.35 lines 32-49); and wherein the transferring the first vector and transferring the second vector include temporarily storing the first vector and the second vector in the first and second buffers (*see Lee 1.3.4, 2.3.2, also see Ch. 5; also see Cooke et al. col.35 lines 32-49 & col.42 lines 55-63)*.

7.8 As per claim 8, the combined teachings of Lee and Cooke et al. substantially teach that the determining the first buffer size comprises determining an associated size of the vector input port, wherein the required size of the buffer is equal to the size of the vector (*see Lee pgs 152-167; and also see Cooke et al. col.35 lines 32-67*).

7.9 With regards to claim 9, the combined teachings of Lee and Cooke et al. substantially teach that the determining the first buffer size comprises determining the first buffer size as a function of a value of a user-provided configuration parameter (*see Lee pgs 152-167; and also see Cooke et al. col.41 line 5-col.42 line 63)*.

7.10 Regarding claim 10, the combined teachings of Lee and Cooke et al. substantially teach that the configuration parameter is associated a buffer-size compilation option of the HLMS *(see Lee pgs.14, 28,80,152-167; also see Cooke et al. col.53 line 20-col.54 line 42)*.

7.11 As per claim 11, the combined teachings of Lee and Cooke et al. substantially teach that one or more input/output ports each has an associated configuration parameter value *(see Lee pg.51-54, 103-106 and 141-151; also see Cooke et al. col.53 line 20-col.54 line 42)*.

7.12 With regards to claim 12, the combined teachings of Lee and Cooke et al. substantially teach estimating FPGA resources available for buffers (*see Lee pgs.11-15; also see Cooke et al. col.41 line 5-col.42 line 63)*; and selecting the first and second buffer sizes as a

function of the estimated available resources (*see Lee pgs. 152-167, 60-65,140; also see Cooke et al. col.41 line 5-col.42 line 63).*

7.13 As per claim 16, the combined teachings of Lee and Cooke et al. substantially teach the step of simulating operation of a third high-level block in the design in a high-level modeling system (HLMS) (*see section 2-3)*; and outputting a sequence of scalar values from a vector of data received by the second high-level block from the first hardware-implemented block to the third high-level block (*see Lee 1.3.4, 2.3.2, also see pg. 141-151,176-178, Ch. 5; also see Cooke et al. col.35 lines 32-49 & col.42 lines 55-63).*

7.14 Regarding claim 17, the combined teachings of Lee and Cooke et al. substantially teach the step of co-simulating a third hardware-implemented block on a hardware co-simulation platform, wherein the third hardware implemented block implements a third high-level block in the design (*see Lee section 2-3, ch.5*); and outputting a sequence of scalar values from a vector of data received by the second high-level block to the third high-level block (*see Lee 1.3.4, 2.3.2, also see pg. 141-151,176-178, Ch. 5;; also see Cooke et al. col.35 lines 32-49 & col.42 lines 55-63).*

Conclusion

8. Claims 1-12,14-17, and 23 are rejected and Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre Pierre-Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

July 24, 2007

APL

ZOILA CABRERA
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100
7/30/07